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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/814,811	03/31/2004	Philippe Messager	A64.12-0004	5300

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WESTMAN CHAMPLIN & KELLY, P.A.
SUITE 1400 - INTERNATIONAL CENTRE
900 SECOND AVENUE SOUTH
MINNEAPOLIS, MN 55402-3319

EXAMINER	
NGUYEN, HIEP	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 02/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/814,811	MESSAGER, PHILIPPE	
	Examiner	Art Unit	
	Hiep Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-5,8-16,21,24 and 25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *21,24 and 25* is/are allowed.

6)☒ Claim(s) *1,3-5,8 and 13-16* is/are rejected.

7)☒ Claim(s) *9-12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The finality of the Office Action filed on 10-13-05 has been withdrawn.

Claim Objections

Claim 1 is objected to because of the following informalities: the recitations "a second transistor" and 'a third transistor" are confusing because it is not clear what is the first transistor. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3 and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Nagata (USP. 5,990,671).

Regarding claim 1, figure 1 of Nagata shows an integrated circuit comprising means delivering to at least one output a predetermined output voltage representative of a logic level, which comprises means of generating a main voltage (VEXT) and means of generating a reference voltage (Vref) lower than the main voltage, characterized in that it comprises

means of connecting the main voltage on the output (Qp3), and

means of limiting and/or detecting (3, 4, 5) the voltage on the output (VINT) at the value of the predetermined output voltage, equal to the reference voltage VREF), and which comprises at least a "second" transistor (Qn3) having a gate connected to the gate of a "third" transistor (Qn1) mounted as a diode at the reference voltage (col. 1, lines 30-48).

Regarding claim 3, transistor (Qp3) is turned on/off to regulate the voltage (VINT). The source of transistor (Qp3) is coupled to the gate of transistor (Qn6) and to capacitor (11). These two elements do not draw current. There are only leakage currents through the gate of

transistor (Qn6) and capacitor (11). Thus, these leakage currents are very small, in the neighborhood of microamps (USP. 5,767,550; US 2005/0169040).

Regarding claim 16, figure 1 of Nagata shows a communication module for an integrated circuit comprising: an output, a predetermined output voltage (VINT), a main voltage (VEXT), a reference voltage (VREF) lower than the main voltage, means for connecting the main voltage to the output (Qp3). Means for limiting the voltage on the output at a predetermined value comprising a first transistor (Qn3) having a gate connected to the gate of a second transistor (Qn1) mounted as a diode at the reference voltage (VREF).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4, 5, 8 and 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagata (USP. 5,990,671).

Regarding claims 4 and 5, figure 1 of Nagata includes all the limitations of claims 4 and 5 except for the limitation that transistor (Qp3) is a power transistor. However, it is old and well known in the art that a power transistor can conduct high current and is used to drive heavy load. Therefore, it would have been obvious for one of ordinary skill in the art to replace transistor (Qp3) with a power transistor for driving a heavy load. The drain of transistor (Qp3) is connected to the output and its source is connected to the main voltage (VEXT).

Regarding claim 8, when the output voltage is reached, a voltage is sent to the gate of transistor (Qp3) to block the increase of current flowing through transistor (Qp3) for keeping the output voltage constant (col. 3 lines (16-29).

Regarding claims 13 and 14, the recitation "a USB connection" and "the logic CMOS section of the integrated circuit" are merely intended use thus; they do not further limit the limitations of the claims. It has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex Parte Masham, 2 USPQ F.2d 1647 (1987). Therefore, these limitations have not been given patentable weight.

Regarding claim 15, figure 1 of Nagata includes all the limitations of claim 15 except for the values of predetermined value (3V) and the main voltage value (5V). However the particular values recited by the applicant are considered to be design expedient depending upon a particular environment or an application in which the circuit of Nagata is to be used. Lacking of showing any criticality, a skilled artisan would be motivated to select predetermined value of (3V) and the main voltage value of (5V) for providing required constant output voltage level.

Allowable Subject Matter

Claims 21, 24 and 25 are allowed because the prior art of records (USP. 5,990,671) fails to teach or suggest an integrated circuit comprising a blocking means having first and second currents mirrors connected to each other.

Claims 9-12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 9-12 would be allowable because the prior art of records (USP. 5,990,671) fails to teach or suggest an integrated circuit comprises a blocking means having first and second current mirror as called for in claims 9 and 10; a first power transistor connected to a command input via a fourth transistor as called fore in claim 11 and the fourth transistor is weaker than the transistors of the second mirror as called for in claim 12.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hiep Nguyen
01-09-06

TUAN T. LAM
PRIMARY EXAMINER